

ABSTRACT

Novel structures and methods for evaluating lines in semiconductor integrated circuits. A first plurality of lines can be formed on a wafer each of which comprises multiple line sections. All the line sections are of the same length. The electrical resistances of the line sections are measured. Then, a first line geometry adjustment is determined based on the electrical resistances of all the sections of all the lines. The first line geometry adjustment represents an effective reduction of cross-section size of the lines due to grain boundary electrical resistance. A second plurality of lines of same length and thickness can be formed on the same wafer. Then, second and third line geometry adjustments can be determined based on the electrical resistances of these lines measured at different temperatures. The second and third line geometry adjustments represent an effective reduction of cross-section size of the lines due to grain boundary electrical resistance and line surface roughness.